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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/847,032	04/30/2001	Lester S. Sanders	X-858 US	5645

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EXAMINER	
PHAN, THAI Q	

ART UNIT	PAPER NUMBER
2128	

DATE MAILED: 08/10/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/847,032	SANDERS, LESTER S.	
	Examiner	Art Unit	
	Thai Phan	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05/05/2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 April 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to applicant's amendment, filed on 05/05/2006. Claims 1-30 are pending in this Action.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-30 are rejected under 35 U.S.C. 102(e) as being anticipated by Bennett et al, US patent no. 5,659,484

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

As per claim 1, Bennett anticipates a method and system for mapping or targeting an integrated circuit placement/layout for circuit components with feature

limitation very identical to the claimed invention. According to Bennett, the method includes steps

Receiving a first low level placed and routed design representation for an integrated circuit, a first circuit, (Figs. 6-7, col. 29, line 34 to col. 30, line 6),

Transforming the low level design representation into a synthesizable, editable, and simulatable high level design representation like HDL or ABEL (col. 10, lines 35-66, Background of the Invention, col. 29, line 34 to col. 30, line 20),

Processing the high level presentation to generate a low level, placed and routed design representation targeting a second integrated circuit that is different from the first integrated circuit by device independent tool sets for targeting the device for simulation and synthesis, code enumeration and annotation to meet the design specification or constraints (col. 10, lines 13-66, col. 11, lines 10-26, col. 15, lines 3-13, col. 29, lines 35-46, cols. 29-30).

As per claims 2-4, Bennett anticipates the design circuits are programmable logic devices including gate array, FPGA, etc.

As per claims 5-8, Bennett anticipates design tools such as HDL programming language, ABEL language, Boolean equation/expression tools, etc. (Fig. 7).

As per claim 9, Bennett anticipates the low level design as Boolean equations (306).

As per claim 10, Bennett anticipates a step of compiling the low level representation to generate an editable and simulatable high-level representation for

timing or delay analysis (col. 5, line 56 to col. 6, line 35, col. 10, lines 50-60, col. 11, lines 3-10, cols. 22-29, for exemplary).

As per claims 11-17, Bennett anticipates the claimed limitations in the process technology mapping for logic gate array design.

As per claim 18, Bennett anticipates VHDL design code for the high-level design representation (Fig. 7, block 306, and cols. 29-30).

As per claims 19-21, Bennett anticipates ABEL, Verilog code and Boolean equations as claimed (Fig. 7).

As per claim 22, Bennett anticipates a method and system for mapping or targeting an integrated circuit placement/layout for circuit components with feature limitation very identical to the claimed invention. According to Bennett, the method includes steps

Receiving or inputting a first low level placed and routed design representation for an integrated circuit, a first circuit, (Figs. 6-7, col. 29, line 34 to col. 30, line 6),

Transforming the low level design representation for generating from the transformed design representation into a synthesizable, editable, and simulatable high level design representation like HDL or ABEL codes (col. 10, lines 35-66, Background of the Invention, col. 29, line 34 to col. 30, line 20),

Processing the high level presentation to generate a low level, placed and routed design representation targeting a second integrated circuit that is different from the first integrated circuit (due to tool sets for targeting device independent) for simulation and synthesis of the targeted device, for code enumeration and annotation to meet the

design specification or constraints (col. 10, lines 13-66, col. 11, lines 10-26, col. 15, lines 3-13, cols. 22-30).

As per claims 23-30, the claims are directed to a method and system for retargeting an electronic design. The claims require the feature limitations, such as programmable logic devices, gate array designs, ASIC design, etc, as shown in the rejected claims above. Claims 23-30 are also rejected in like manner.

Response to Arguments

Applicant's arguments filed 05/05/2006 have been fully considered but they are not persuasive.

In response to applicant's argument Bennett does not teach transforming placement and routing in a low level design into a synthesizable high level design (page 6, paragraph 4), the examiner disagrees with. Bennett discloses the claimed transforming the placed and routed in a low level design using design capture step (304) into an editable, simulatable and/or synthesizable high level format (col. 29, line 35 to col. 30, line 20).

In response to applicant's argument Bennett does not teach or disclose targeting a first integrated circuit and targeting a second integrated circuit that is different from the first (page 6, paragraph 5), the examiner responds Bennett discloses such feature, for example, the devices independent logic synthesis tools (col. 29, lines 41-46) targeting different and independent devices. In other words, the device independent tool sets target different devices for simulation and/or synthesis (Fig. 7, col. 29, lines 34-66).

Conclusion

3. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

1. US patent no. 6,035,106, issued to Carruthers et al, on March 2000

2. US patent no. 6,763,506, issued to Betz et al, on July 2004

4. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thai Phan whose telephone number is 571-272-3783. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamini Shah can be reached on 571-272-2279. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

6. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Aug. 02, 2006

Thai Phan
Patent Examiner